IN THE CLAIMS

Please amend the claims as follows:

1. (original) Phase-switching dual modulus prescaler, comprising a dual modulus divider (10) comprising:

- a first and second divide-by-2 circuit (A;B), wherein said second divide-by-2 circuit (B) is coupled to the output of said first divide-by-2 circuit (A) and at least said second divide-by-two circuit (B) comprises four phase outputs (I_p, I_n, Q_p, Q_n; INi, INni, INq, INnq) each separated by 90°;

- a phase selection unit (PSU) for selecting one of the four phase outputs (I_p, I_n, Q_p, Q_n; INi, INni, INq, INnq) of the second divide-by-2 circuit (B);

- a phase control unit (RTU) for providing control signal (C1, NC0; C2, NC2; C3, NC3) to the phase selection unit (PSU), wherein the phase selection unit (PSU) performs the selection of the four phase outputs (I_p, I_n, Q_p, Q_n; INi, INni, INq, INnq) according to the control signals (C0, NC0; C1, NC1; C2, NC2); and

- said phase selection unit (PSU) is implemented based on direct logic.

2. (original) Prescaler according to claim 1, wherein

- the output (OUT) of the phase selection unit (PSU) is implemented according to the following logic code:

$$OUT = \overline{NC0 \bullet NC1 \bullet INi} + \overline{NC0 \bullet C1 \bullet INni} + \overline{C0 \bullet NC2 \bullet INnq} + \overline{C0 \bullet C2 \bullet INq} \ ,$$

- $+, \bullet, \overline{}$ represent an OR-, AND, and NAND functions, respectively.

3. (currently amended) Prescaler according to claim 1~~ or 2~~, further comprising

- a divide-by-4 circuit (UA) coupled to the output of the phase selection unit (PSU), said divide-by-4 circuit (UA) comprises a sixth and seventh divide-by-2 circuit (F, G) each with four phase outputs (I_p, I_n, Q_p, Q_n) separated by 90°, said seventh divide-by-2 circuit (G) being coupled to the quadrature output (Qp, Q_n) of the sixth divide-by-2.

4. (currently amended) Prescaler according to claim 1~~, 2 or 3~~, wherein

- the phase control unit (RTU) comprises a fourth and fifth divide-by-2 circuit (D, E) each with four phase outputs (I_p, I_n, Q_p, Q_n) separated by 90°, said fourth and fifth divide-by-2 circuit (D, E) being coupled in series,

- the In-phase output signal (I_p, I_n) of the fifth divide-by-2 circuit (E) corresponds to the control signal (C0),
- the In-phase output signal (I_p, I_n) of the fourth divide-by-2 circuit (D) corresponds to the control signal (C1),
- the quadrature phase output signal (Q_p, Q_n) of the fourth divide-by-2 circuit (E) corresponds to the control signal (C2).

5. (original) Prescaler according to claim 4, wherein
- the phase control unit (RTU) further comprises a D-latch (DL) coupled to the input of the fifth divide-by-2 circuit (E),
- the D-latch (DL) receives the previous state of the In-phase output (Ip, I_n) of the seventh divide-by-2 circuit (G) and a signal (modul) indicating the number of phase switching as input signals.

6. (original) Prescaler according to claim 1, wherein said dual modulus divider (10) is a 16/17 divider.

7. (original) Prescaler according to claim 1, further comprising a synchronization loop coupled to the dual modulus divider (10) for reclocking the dual modulus divider (10).

8. (currently amended) Frequency synthesizer comprising a prescaler according to ~~any one of the claims 1 to 7~~claim 1.